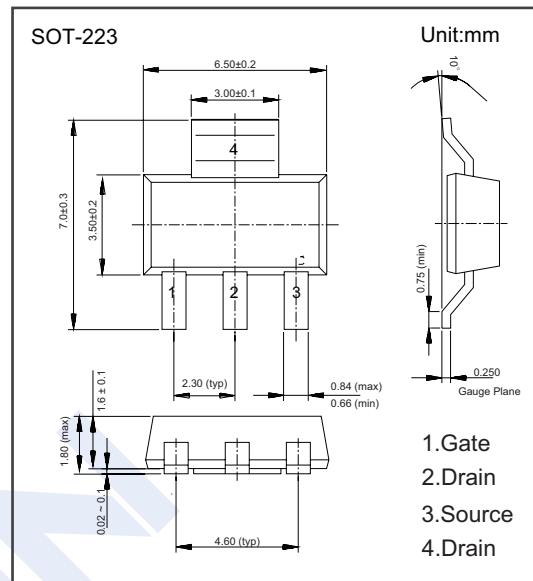
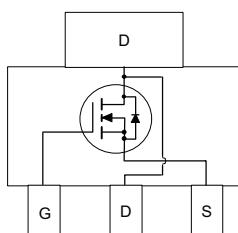


N-Channel MOSFET

FDT457N

■ Features

- 5 A, 30 V. $R_{DS(ON)} = 0.06 \Omega$ @ $V_{GS} = 10$ V
 $R_{DS(ON)} = 0.09 \Omega$ @ $V_{GS} = 4.5$ V.
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.

■ Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	V_{DS}	30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current (Note 1a)	I_D	5	A
Pulsed Drain Current	I_{DM}	16	
(Note 1a)		3	W
Power Dissipation (Note 1b)	P_D	1.3	
(Note 1c)		1.1	
Thermal Resistance.Junction- to-Ambient (Note 1a)	R_{thJA}	42	$^\circ\text{C}/\text{W}$
Thermal Resistance.Junction- to-Case (Note 1)	R_{thJC}	12	
Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to 150	

Notes:

1. R_{thJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{thJC} is guaranteed by design while R_{thCA} is determined by the user's board design.
 - a. $42^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2oz Cu.
 - b. $95^\circ\text{C}/\text{W}$ when mounted on a 0.066 in² pad of 2oz Cu.
 - c. $110^\circ\text{C}/\text{W}$ when mounted on a 0.00123 in² pad of 2oz Cu.

N-Channel MOSFET**FDT457N**

■ Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

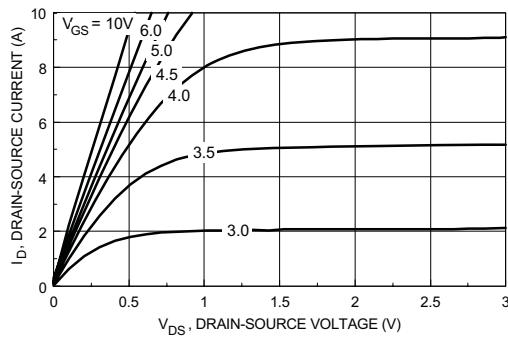
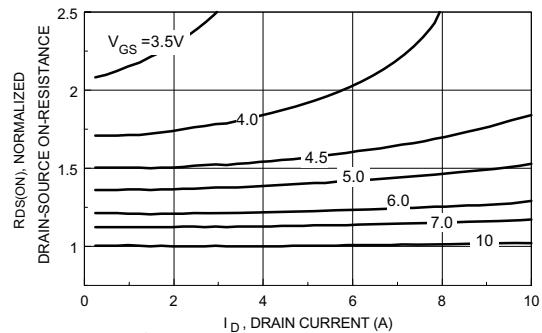
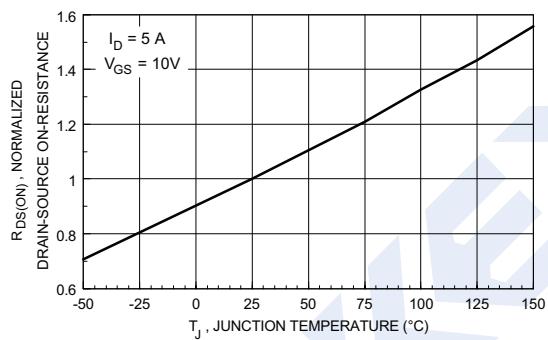
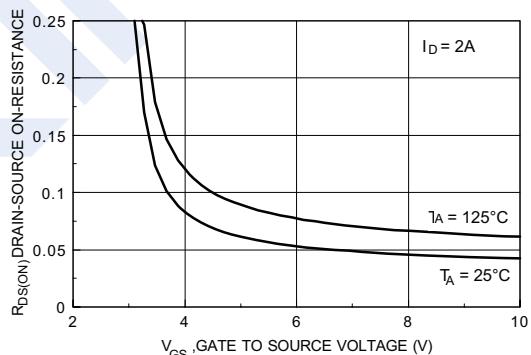
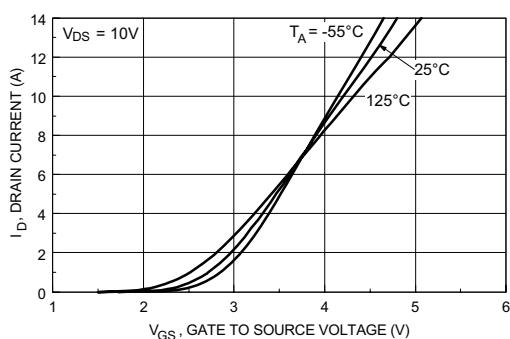
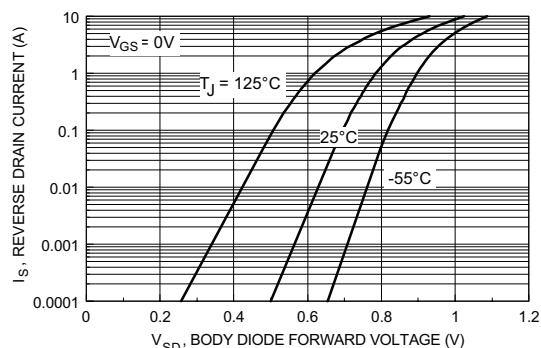
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	$I_D=250 \mu\text{A}, V_{GS}=0\text{V}$	30			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=24\text{V}, V_{GS}=0\text{V}$		1		μA
		$V_{DS}=24\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$		10		
Gate-Body Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS}=V_{GS}, I_D=250 \mu\text{A}$	1		3	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=10\text{V}, I_D=5 \text{ A}$			0.06	Ω
		$V_{GS}=10\text{V}, I_D=5 \text{ A}, T_J=125^\circ\text{C}$			0.1	
		$V_{GS}=4.5\text{V}, I_D=3.8 \text{ A}$			0.09	
On State Drain Current	$I_{D(\text{ON})}$	$V_{GS}=10 \text{ V}, V_{DS}=5\text{V}$	5			A
Forward Transconductance	g_{FS}	$V_{DS}=10\text{V}, I_D=5\text{A}$		5		S
Input Capacitance	C_{iss}	$V_{GS}=0\text{V}, V_{DS}=15\text{V}, f=1\text{MHz}$		235		pF
Output Capacitance	C_{oss}			145		
Reverse Transfer Capacitance	C_{rss}			50		
Total Gate Charge	Q_g	$V_{GS}=5\text{V}, V_{DS}=10\text{V}, I_D=5\text{A}$		4.2	5.9	nC
Gate Source Charge	Q_{gs}			1.3		
Gate Drain Charge	Q_{gd}			1.7		
Turn-On DelayTime	$t_{d(on)}$	$V_{GS}=10\text{V}, V_{DD}=10\text{V}, I_D = 1\text{A}, R_{GEN}=6 \Omega$		5	10	ns
Turn-On Rise Time	t_r			12	22	
Turn-Off DelayTime	$t_{d(off)}$			12	22	
Turn-Off Fall Time	t_f			3	8	
Maximum Body-Diode Continuous Current	I_s				2.5	A
Diode Forward Voltage	V_{SD}	$I_s=2.5\text{A}, V_{GS}=0\text{V}$ (Note 2)			1.2	V

Notes:

2. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$

N-Channel MOSFET**FDT457N**

■ Typical Characteristics

**Figure 1. On-Region Characteristics.****Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.****Figure 3. On-Resistance Variation with Temperature.****Figure 4. On-Resistance Variation with Gate-to-Source Voltage.****Figure 5. Transfer Characteristics.****Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

N-Channel MOSFET

FDT457N

■ Typical Characteristics

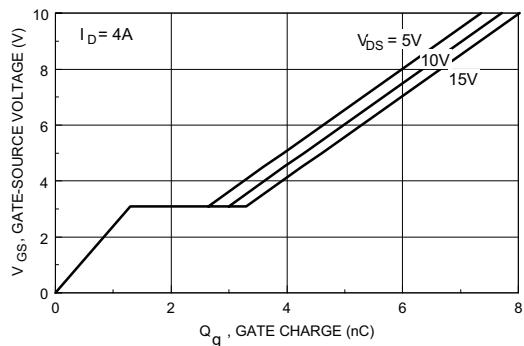


Figure 7. Gate Charge Characteristics.

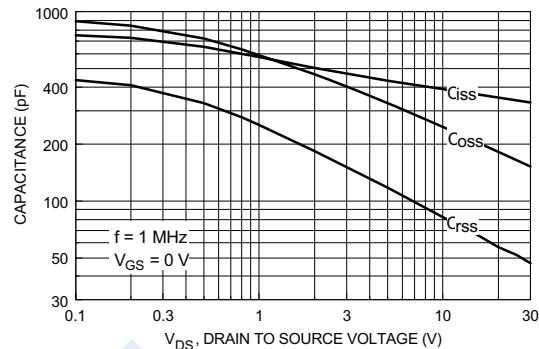


Figure 8. Capacitance Characteristics.

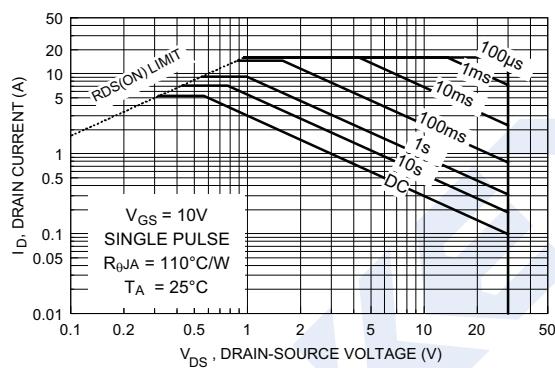


Figure 9. Maximum Safe Operating Area.

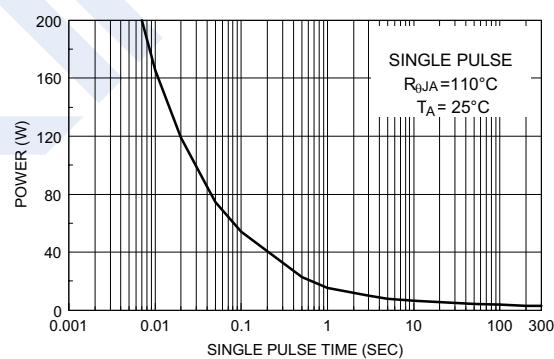


Figure 10. Single Pulse Maximum Power Dissipation.

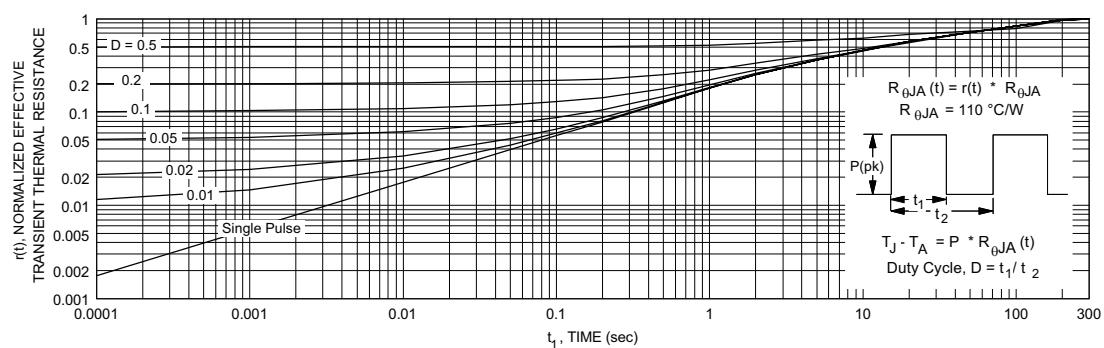


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1c.
Transient thermal response will change depending on the circuit board design.